Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A0**
2. **B0**
3. **O0**
4. **A1**
5. **B1**
6. **O1**
7. **GND**
8. **O3**
9. **B3**
10. **A3**
11. **O2**
12. **B2**
13. **A2**
14. **VCC**

**.043”**

**.043”**

**1 14 14 13**

**12**

**11**

**10**

**9**

**6 7 7 8**

**2**

**3**

**4**

**5**

**F86 A**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: F86A**

**APPROVED BY: DK DIE SIZE .043” X .048” DATE: 3/5/18**

**MFG: TEXAS / FAIRCHILD THICKNESS .015” P/N: 54F86**

**DG 10.1.2**

#### Rev B, 7/19/02